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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,510	01/30/2004	Michael Eneboe	01-490/1C	8371

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EXAMINER	
TO, TUYEN P	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,510	ENEBOE ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	FT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This final office action is in response to the amendment and remarks filed on 02/13/2006. Claims 1-12 remain pending. Claims 13-20 have been canceled.

Terminal Disclaimer

1. The terminal disclaimer filed on 02/13/2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the patents [6,751,783] and [6,026,226] have been reviewed and are accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Patent No. 6,539,531) in view of Wong (US Pub. No. 2002/0113619).

Referring to claim 1, Miller et al. disclose a method for designing an integrated circuit, comprising:

receiving data specifying a plurality of interconnects and components of a design of an integrated circuit (Miller et al. , see fig. 6, figs. 11-23; col. 5 , line 66 to col.6 ,line 31; col. 8 to col. 10); and

However, **Miller et al. do not disclose** the step of optimizing the design of the integrated circuit, wherein data specifying the plurality of interconnects and devices of

an integrated circuit is optimized based on at least one of latency, scalability or isochronous interconnect configuration.

Wong discloses the step of optimizing the design of the integrated circuit, wherein data specifying the plurality of interconnects and devices of an integrated circuit is optimized based on at least one of latency, scalability, or isochronous interconnect configuration (Fig. 12, page 7, paragraphs [0070]-[0072], see "latency").

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Miller et al. with the method disclosed by Wong because such modification includes optimizing the design of the integrated circuit based on latency would provide an efficient interconnect net work architecture by which routing through the resulting interconnect network is guaranteed and that the timing constraints of the interconnect network are predictable (Wong, paragraph [0006]).

Referring to claim 2, the method as described in claim 1, wherein the optimized data is programmed into a self-programmable integrated circuit so as to provide the designed integrated circuit (Wong, Fig. 12, page 7, paragraphs [0070]-[0075], page 1 paragraphs [0007]-[0008]).

Referring to claim 3, the method as described in claim 1, wherein the optimized data is utilized to synthesize an integrated circuit having the specified design (Miller et al., Fig. 6; col. 10, line 35 to col. 12, line 41).

Referring to claim 4, the method as described in claim1, wherein the optimized design includes a specified characteristic for the interconnect, wherein the specified

characteristic includes at least one of latency or scalability (Wong, Fig. 12, page 7, paragraphs [0070]-[0072], see "latency").

Referring to claim 5, the method as described in claim 1, wherein a direct connectivity definition, derived the optimized data, is utilized to synthesize an integrated circuit (Wong, Fig. 12, paragraphs [0008] and [0070]-[0074]).

Referring to claim 6, the method as described in claim 1, wherein optimizing includes at least one of arranging components of the integrated circuit and specifying bandwidth between components (Miller et al., col. 13, lines 21-67; Figs. 8-13; col. 14-16).

Referring to claim 7, the method as described in claim 1, wherein optimizing is performed without user intervention by an agent (Wong, Fig. 12, p. 7, paragraphs [0070]-[0074]).

Referring to claim 8, the method as described in claim 1, wherein the integrated circuit is at least one of an application specific integrated circuit (ASIC) and multiple application specific integrated circuits (ASICs) (Wong, p. 7, paragraph [0075]).

Referring to claim 9, the method as described in claim 1, wherein interconnects not specified by a user are automatically configured by an agent (Miller, Fig. 6, lines 23-56).

4. **Claims 10-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch (US Patent No. 5,829,031) in view of Wong (US Pub. No. 2002/0113619).

Referring to claim 10, Lynch discloses a self-programmable integrated circuit, comprising:

a processor suitable for performing a program of instructions, the processor accessible via a first interconnect (Lynch , Figs. 1-1A; col. 3, line 53 to col. 7, line 29);

at least two components of the integrated circuit, the components communicatively connected via a second interconnect (Lynch , Figs. 1-1A; col. 3, line 53 to col. 7, line 29); and a memory suitable for storing a program of instructions (Lynch, Figs. 1-1A, element 22, col. 3, line 53 to col. 7, line 29), wherein the program of instructions configures the processor to optimize the integrated circuit based on heuristic data indicating past utilization of components of the integrated circuit (Lynch , Figs. 1-1A; col. 3, line 53 to col. 7, line 29, abstract, col. 2, line 12 to col. 3, line 16),

However, Lynch does not disclose wherein the heuristic data is optimized based on at least one of bandwidth, latency, scalability, and isochronous interconnect configuration.

Wong discloses optimizing the design of the integrated circuit, wherein data specifying the plurality of interconnects and devices of an integrated circuit is optimized based on at least one of latency, scalability, or isochronous interconnect configuration (Fig. 12, page 7, paragraphs [0070]-[0072], see "latency").

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Lynch with the method disclosed by Wong because such modification includes optimizing the design integrated circuit (IC) based on latency would provide a designed IC with an efficient interconnect net work architecture by which routing through the resulting interconnect network is guaranteed and that the

timing constraints of the interconnect network are predictable (Wong, paragraph [0006]).

Referring to claim 11, the self-programmable integrated circuit as described in claim 10, wherein the components include at least one of a core, functional block and logical block (Lynch, Figs. 1-1A, elements 28A, 28B, or 30).

Referring to claim 12, the self-programmable integrated circuit as described in claim 10, wherein the heuristic data includes data indicating amount of data transferred between a first component and a second component over the second interconnect (Wong, paragraphs [0038] and [0061]).

5. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

VUTHE SIEK
PRIMARY EXAMINER